

High DR ADC for LHC

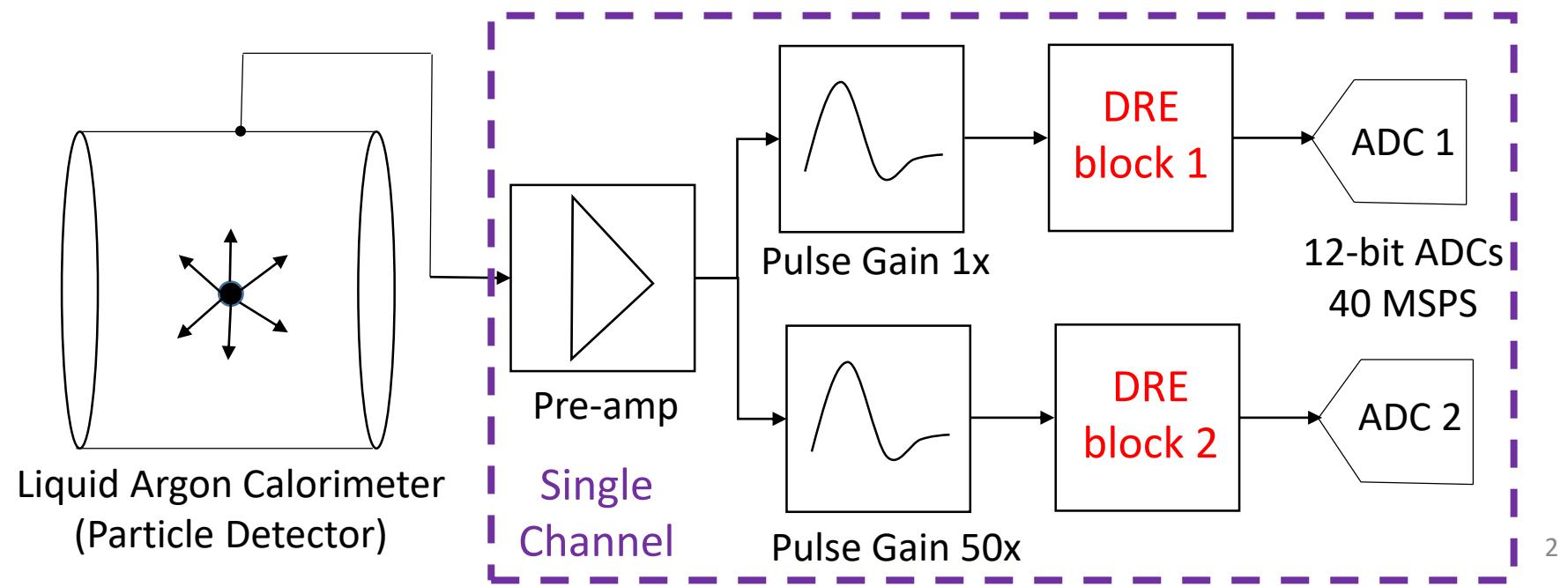
Sarthak Kalani

Last updated: 11/02/16

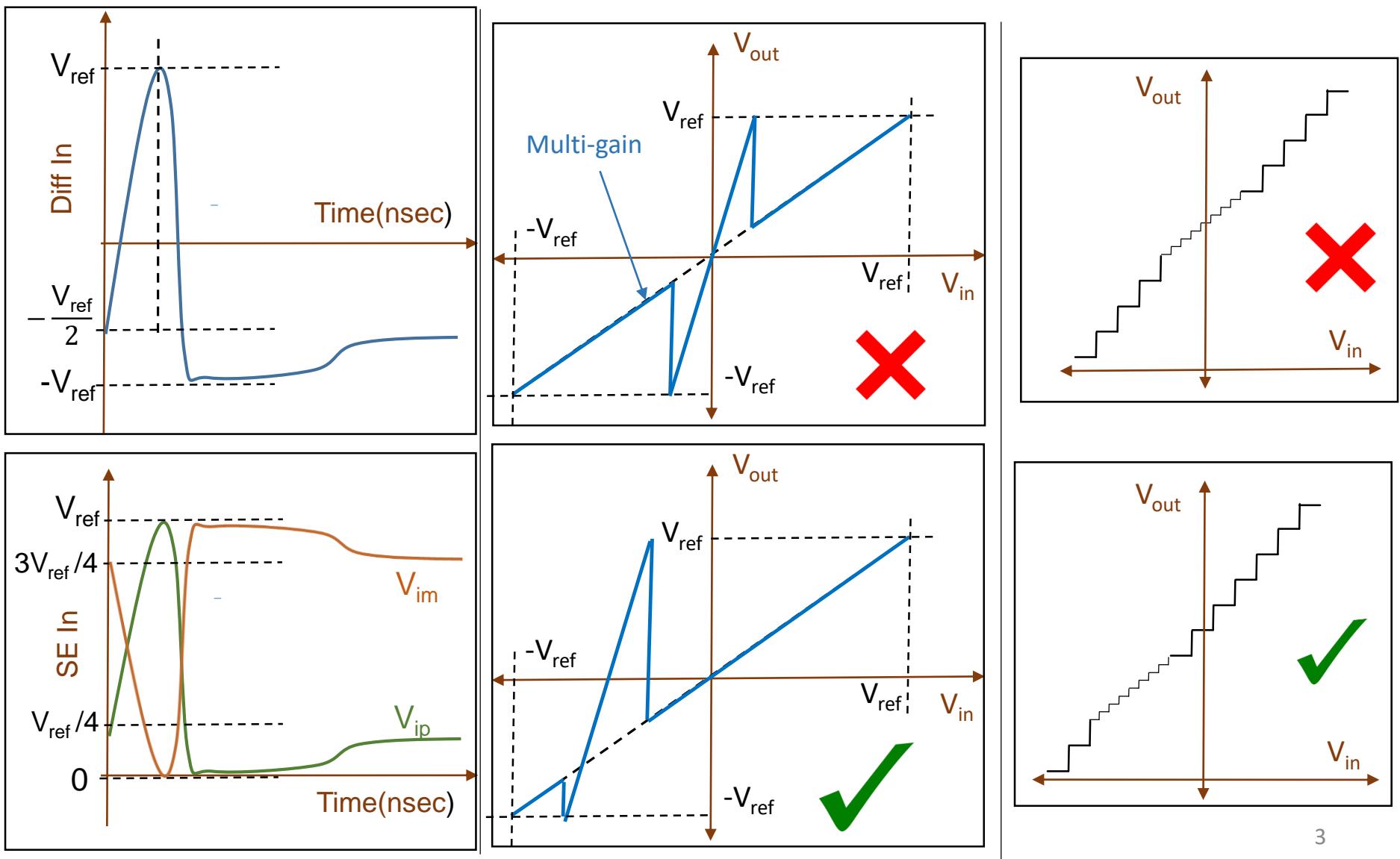


Aim: ADC design for The LHC (Large Hadron Collider), CERN

- ADC specifications:
 - 14-bit design: To accommodate high dynamic range (16 bit)
 - 40MSps
- To design: intermediate block
 - Increase accuracy to 14 bit (or enhance the dynamic range)

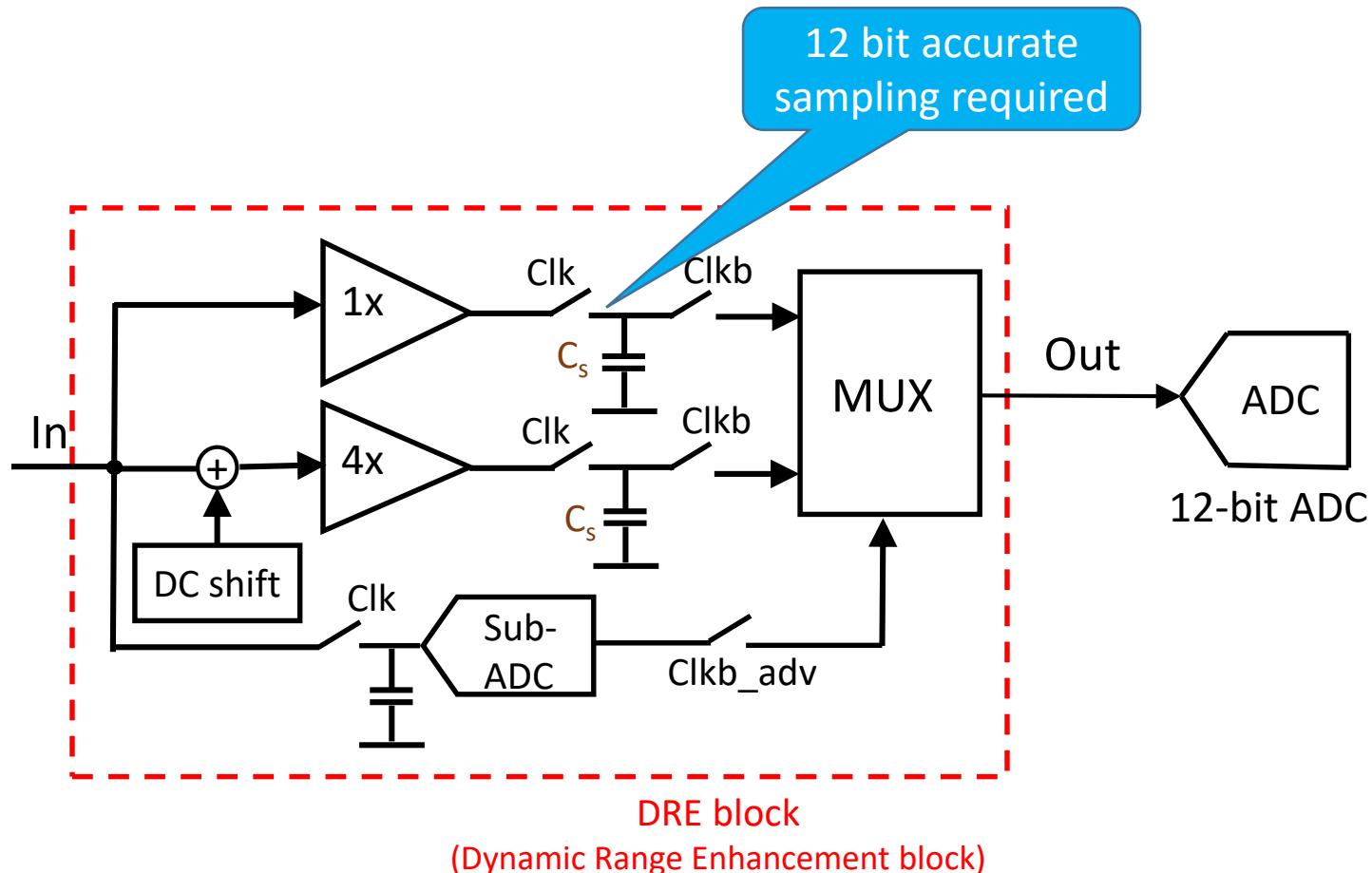


Revisiting requirements: DC shift

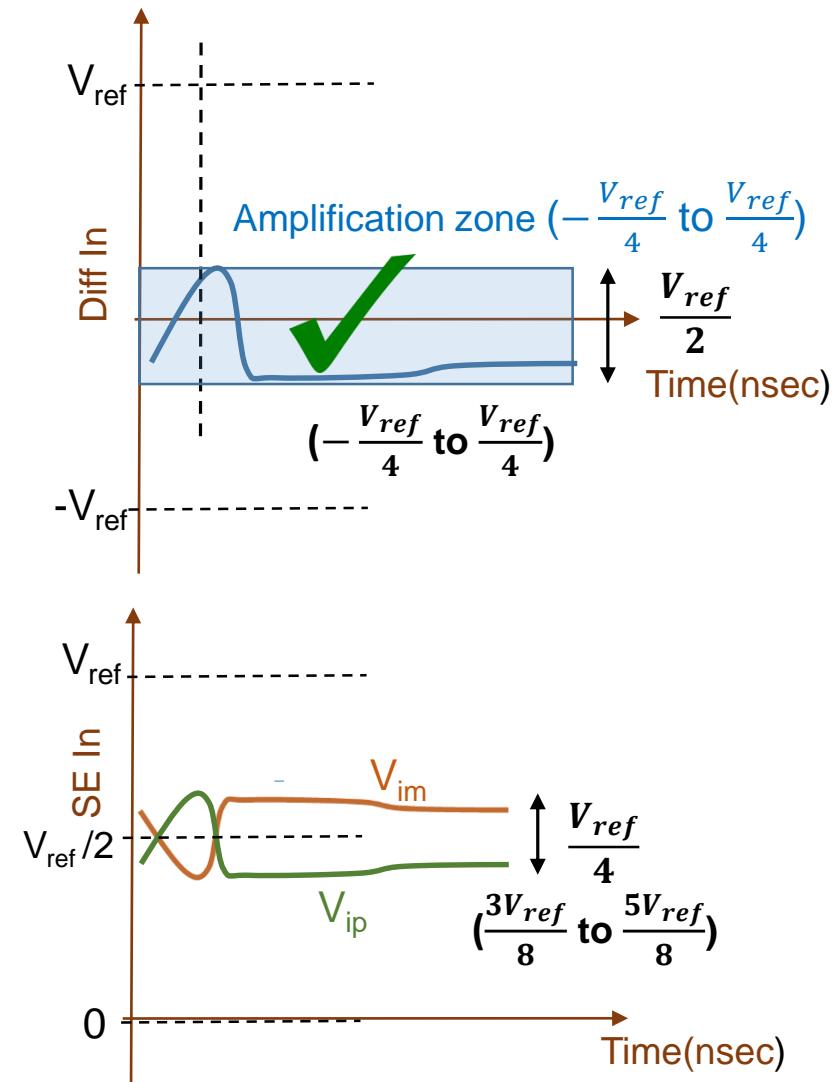
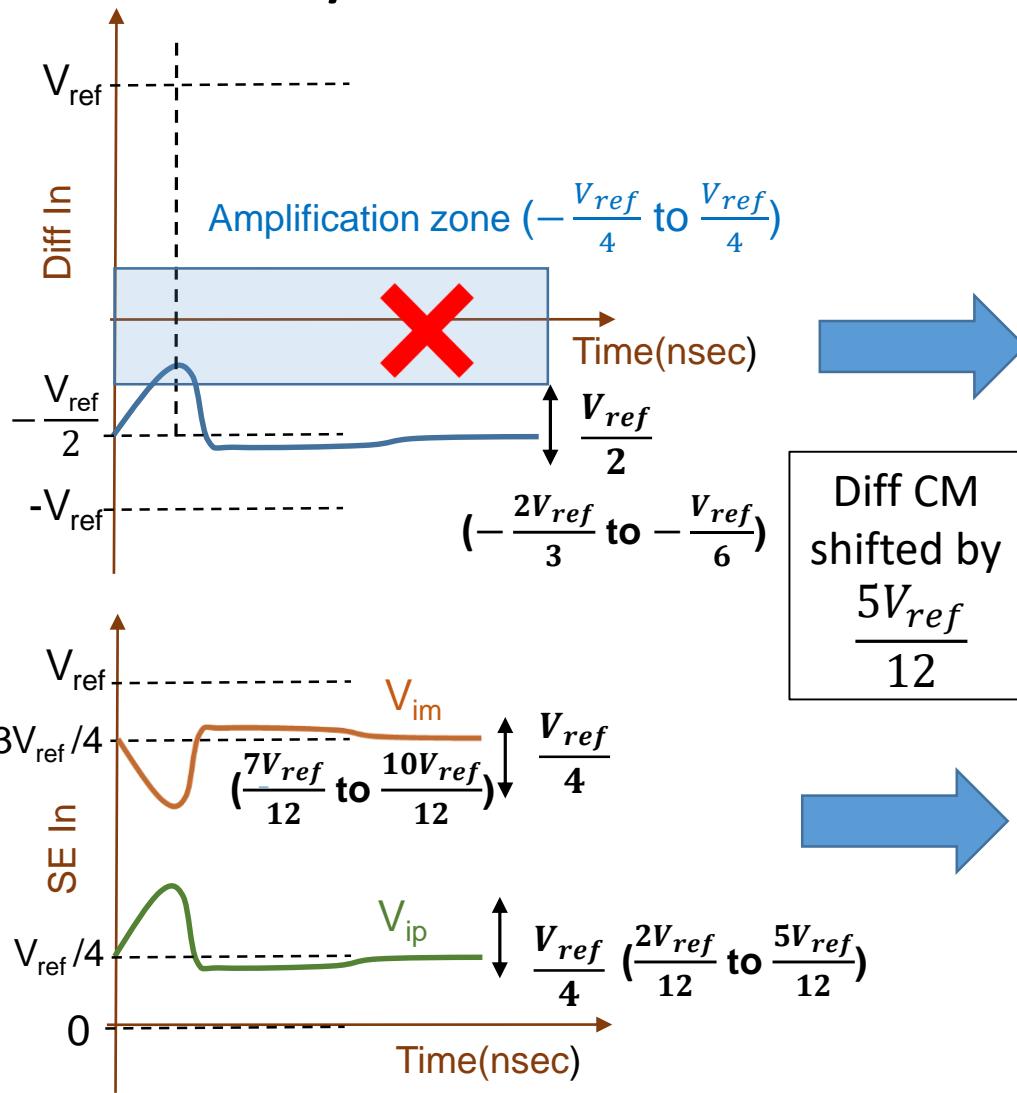


Proposed architecture: Concept

12-bit accurate sampling after analog gain
& dc shift for 4x gain

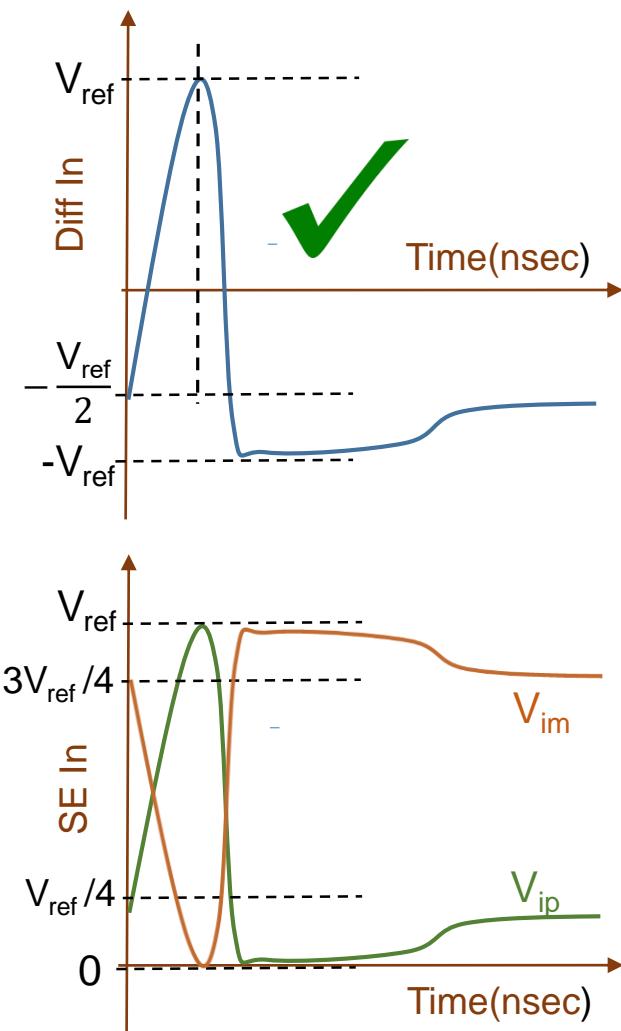


Why shift dc in 4x gain branch?

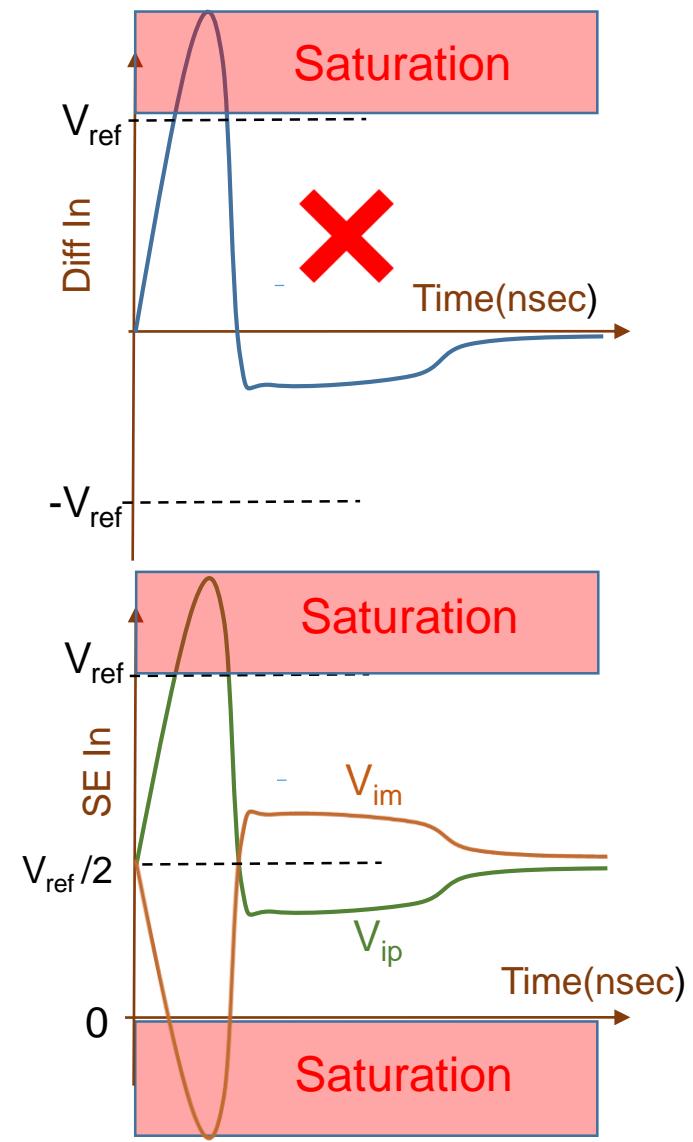


Shift needed to provide amplification in correct zone

Why not shift dc in 1x branch?

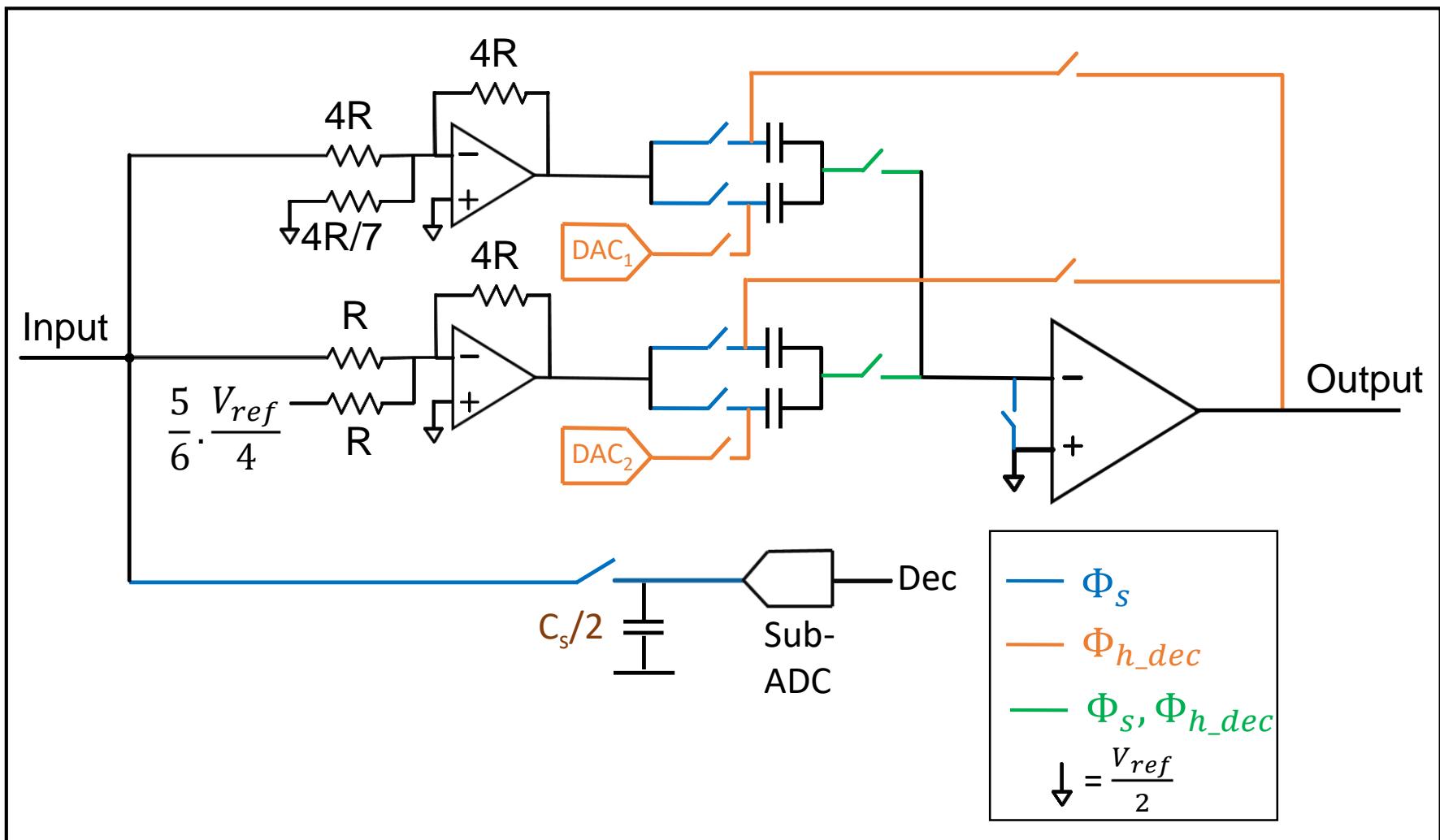


DC Shift



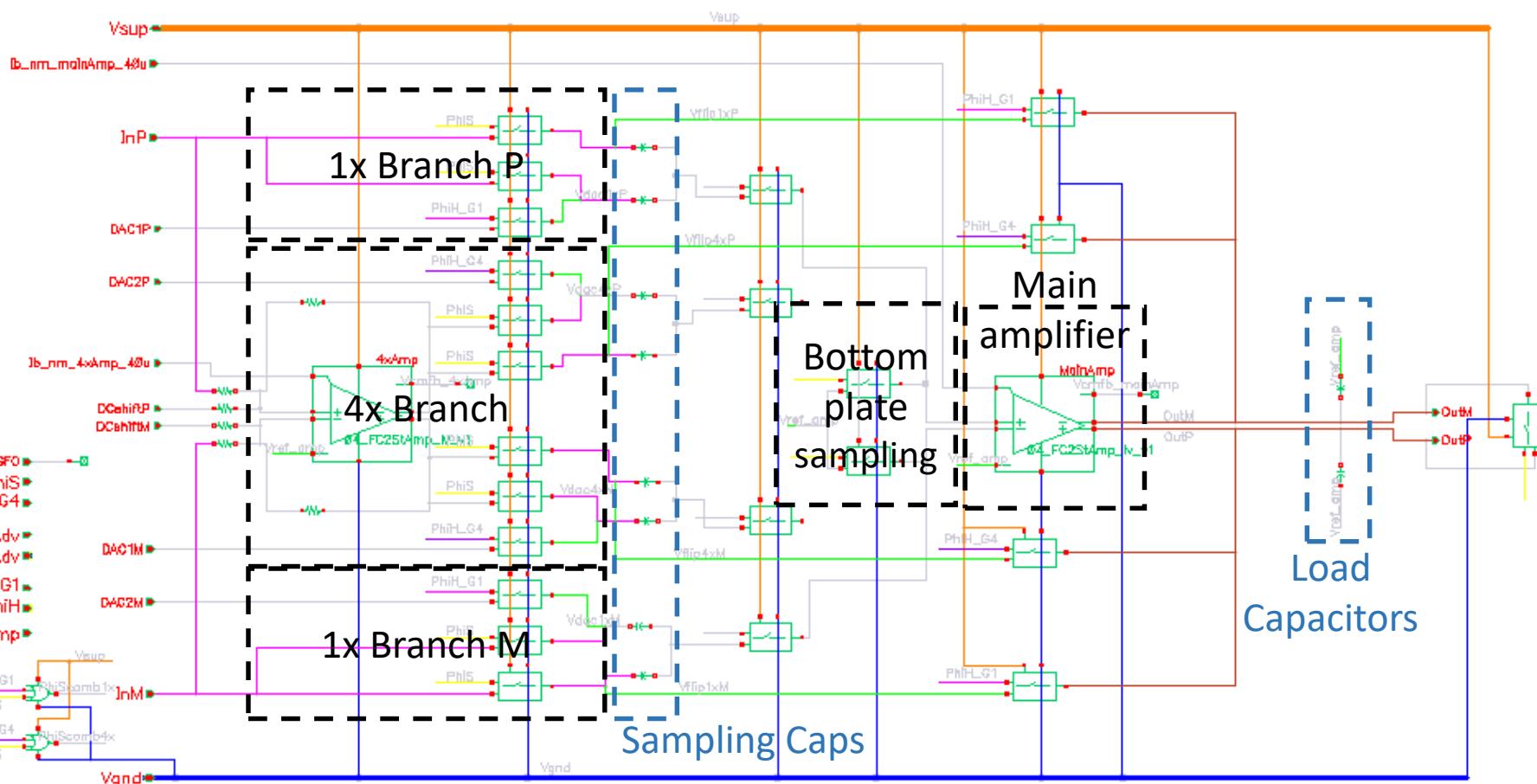
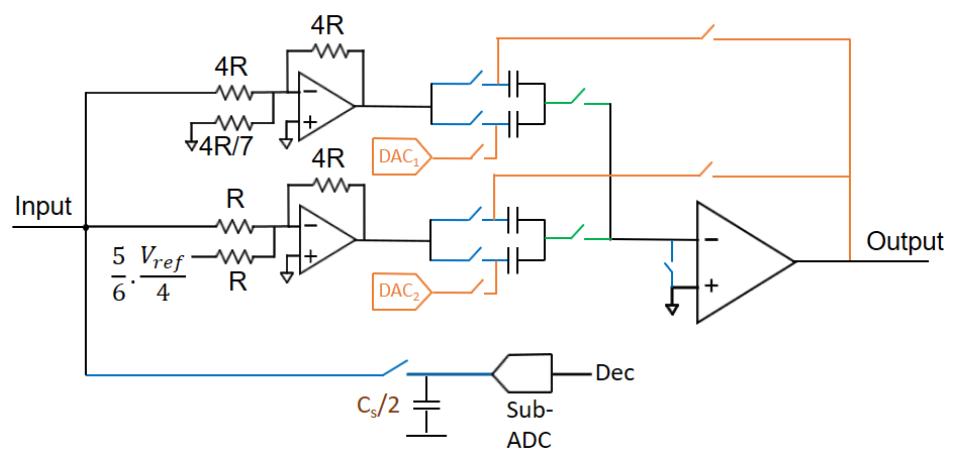
Input will saturate if dc is shifted

Modified multigain architecture (MMG)



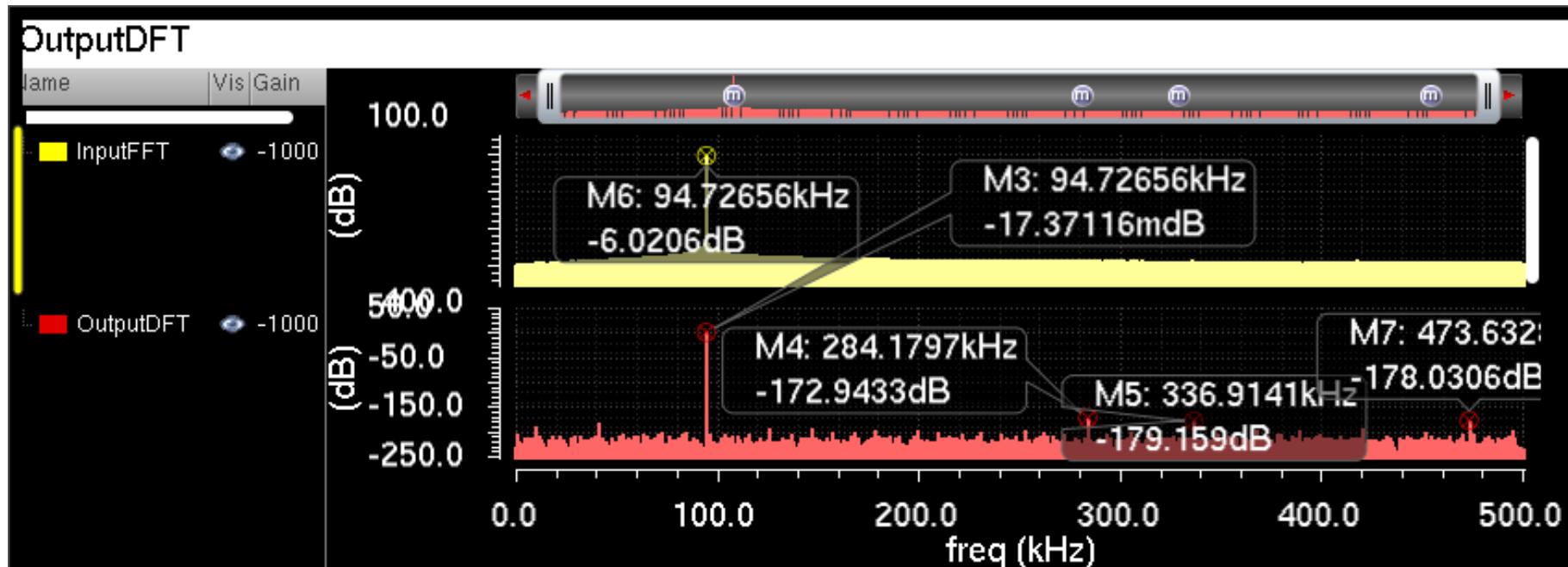
Simulation results

Schematic diagram



Ideal Switches, Ideal Amplifier

1x branch selected, 4x branch disconnected



FFT parameters:

Sampling frequency = 1MHz

Input frequency = $97 \times 1\text{MHz} / 1024 = 94.72\text{kHz}$

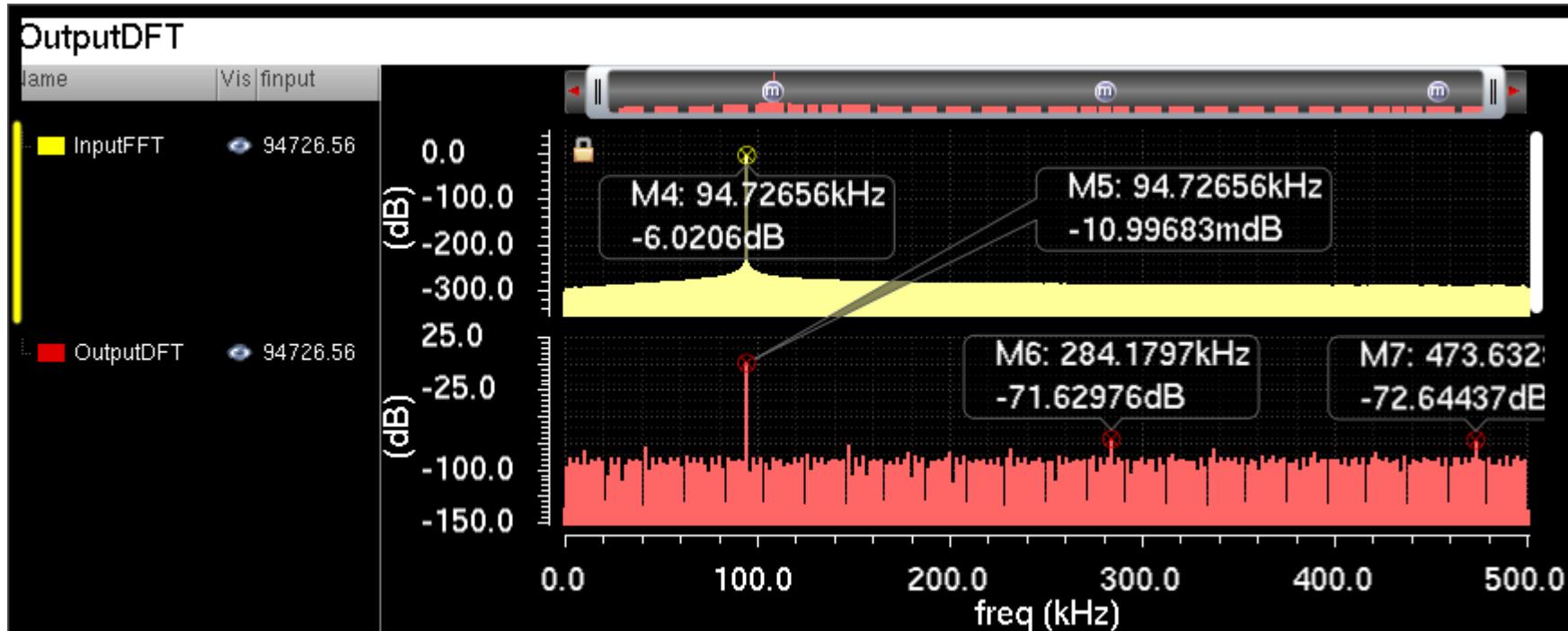
Input Amplitude = 0.5V_{pp} differential

FFT output result:

- Fundamental Tone: -17.37dBV
(expected, for G = 1000 case)
- 3rd harmonic: -172dBV
- 5th harmonic: -178dBV

Real Switches, Real Amplifier

1x branch selected, 4x branch disconnected



FFT parameters:

Sampling frequency = 1MHz

Input frequency = $97 * 1\text{MHz} / 1024 = 94.72\text{kHz}$

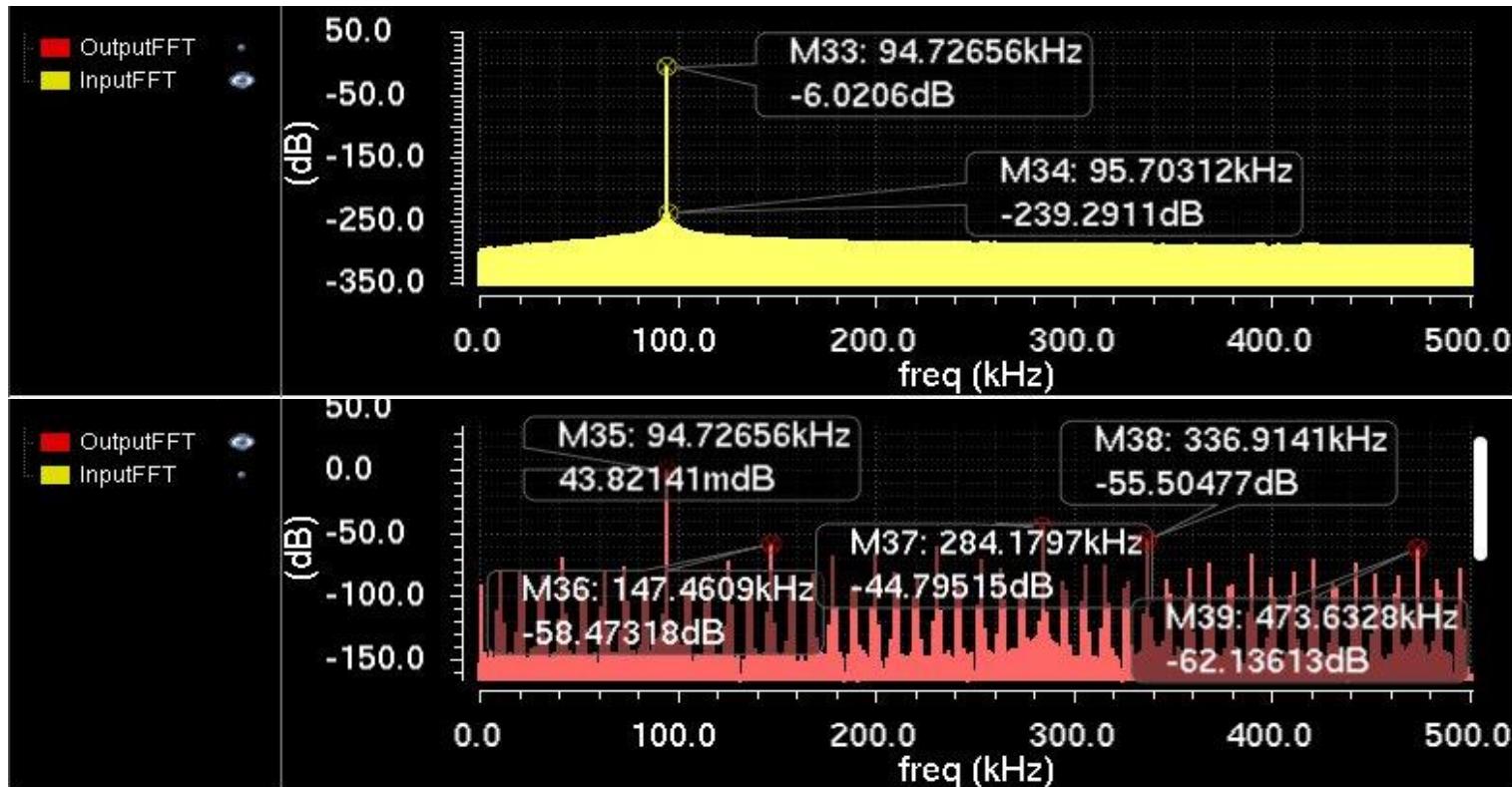
Input Amplitude = 0.5V_{pp} differential

FFT output result:

- Fundamental Tone: -10.99dBV
(expected, for G > 1000 case)
- 3rd harmonic: -71.63dBV
- 5th harmonic: -72.64dBV

Real Switches, Real Amplifier

1x branch selected, 4x branch connected



FFT parameters:

Sampling frequency = 1MHz

Input frequency = $97 \times 1\text{MHz} / 1024 = 94.72\text{kHz}$

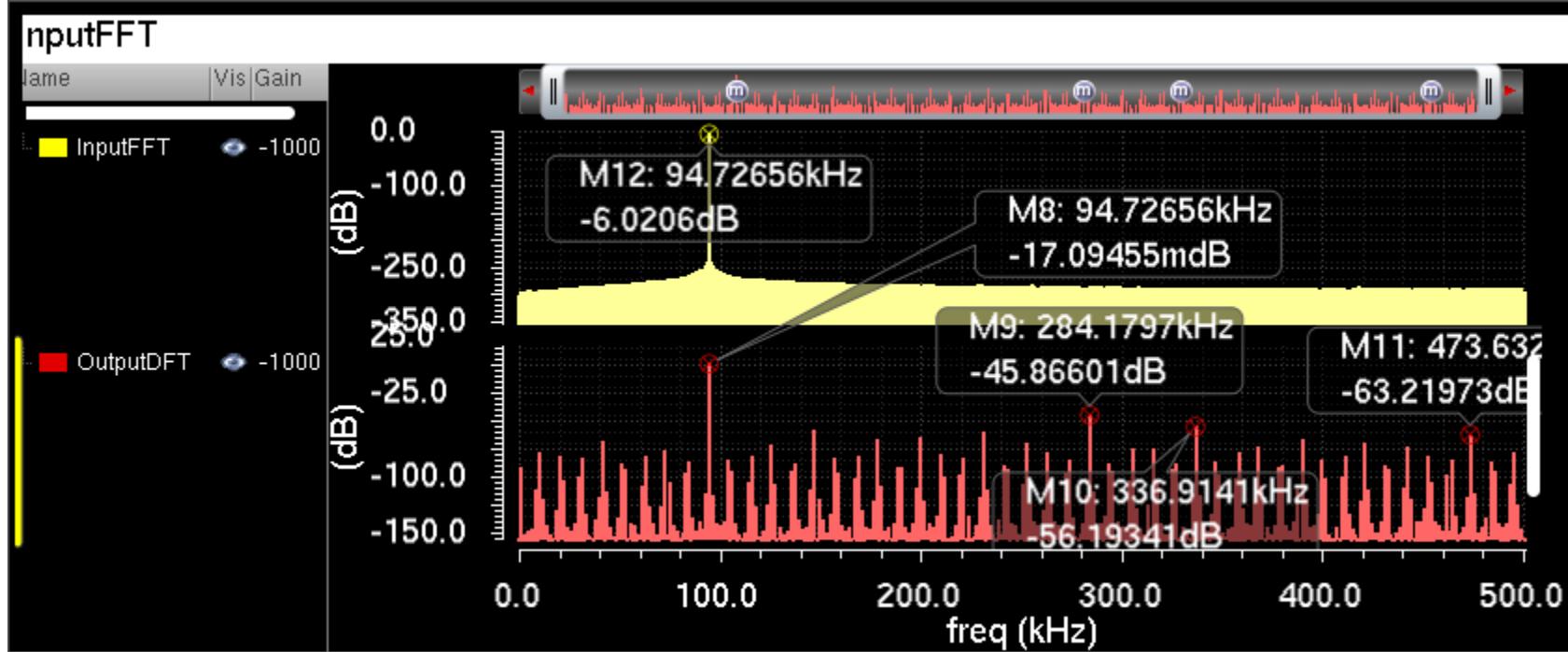
Input Amplitude = 0.5V_{pp} differential

FFT output result:

- Fundamental Tone: **-43.8dBV**
(expected, for G ~ 400 case)
- 2nd harmonic: **-59.4dBV**
- 3rd harmonic: **-44.7dBV**
- 5th harmonic: **-62.1dBV**

Ideal Switches, Ideal Amplifier

1x branch selected, 4x branch connected



FFT parameters:

Sampling frequency = 1MHz

Input frequency = $97 * 1\text{MHz} / 1024 = 94.72\text{kHz}$

Input Amplitude = 0.5V_{pp} differential

FFT output result:

- Fundamental Tone: **-17.09dBV**
(expected, for G = 1000 case)
- 3rd harmonic: **-45.86dBV**
- 5th harmonic: **-63.2dBV**

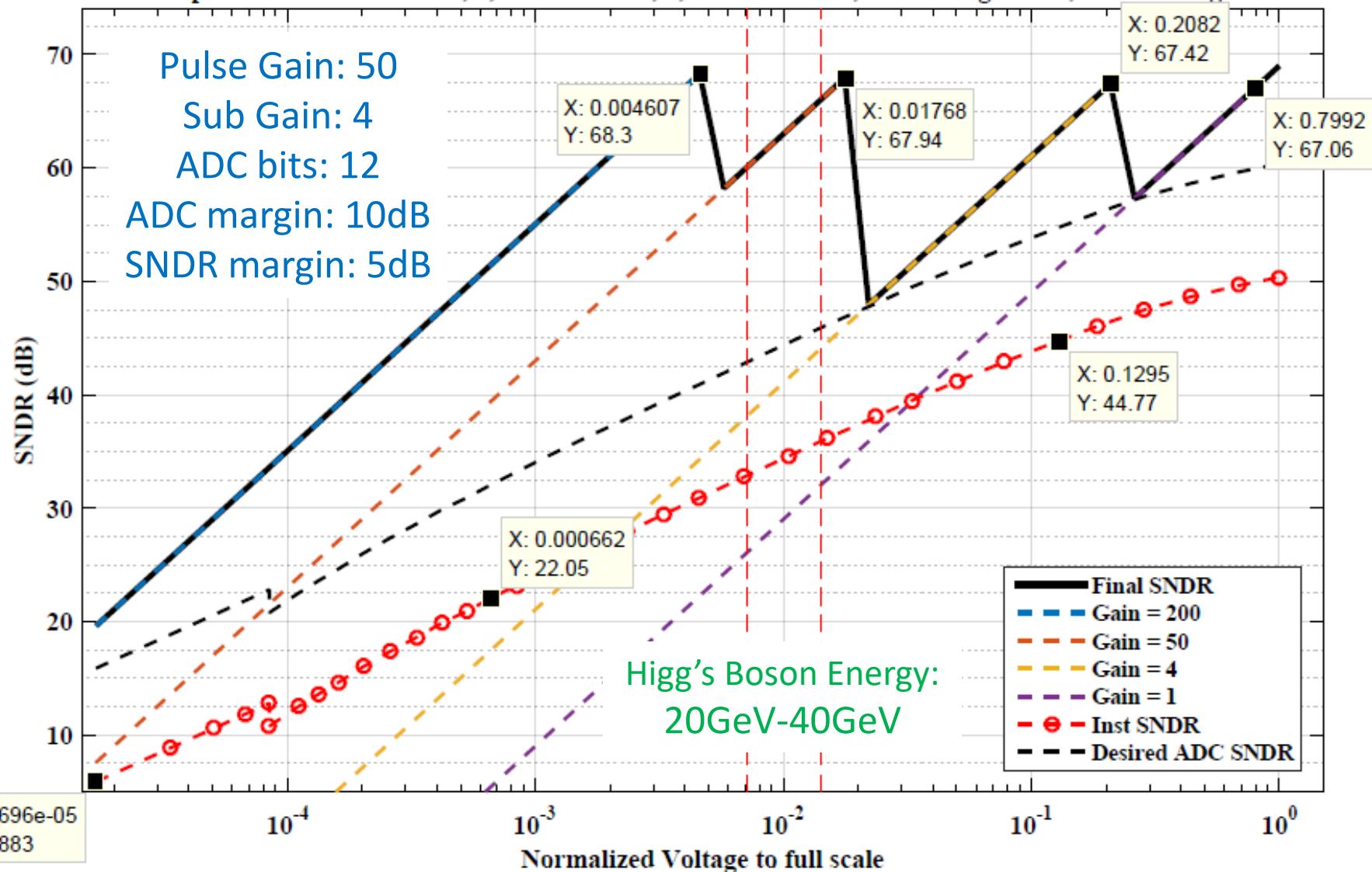
Further plans

- Currently working on
 - Debugging why distortion is 30dB worse on connecting 4x branch.
- Later:
 - SNDR simulation on complete structure.
 - Increase sampling speed.
 - Possibly modify Opamp architecture to improve linearity.

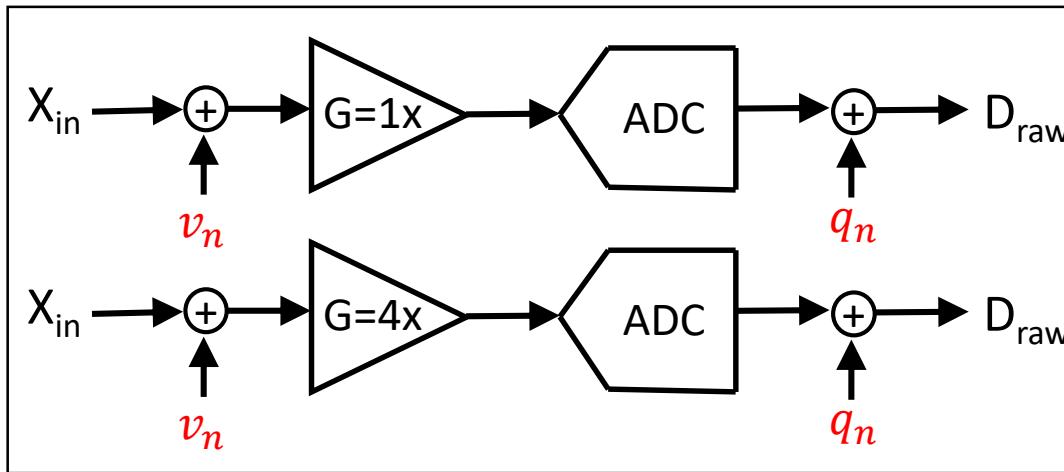
Backup slides

System level SNDR overview

SNDRplot for Pulse Gain = 50, 1, Sub Gain = 4, 1, ADC bits = 12, ADC margin = 10, SNDR margin = 5



Basic noise analysis



$$D_{out} = \frac{D_{raw}}{G} = \frac{G(X_{in} + v_n) + q_n}{G}$$

$\xrightarrow[G=1x]{}$ $D_{out} = (X_{in} + v_n) + q_n$
 $\xrightarrow[G=4x]{}$ $LSB = 12 \text{ bit}$
 $D_{out} = (X_{in} + v_n) + \frac{q_n}{4} - \frac{V_r}{2}$
 $LSB = 14 \text{ bit}$ For dc shift